

ESP32 ECO V3

User Guide



Version 1.0
Espressif Systems
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About This Guide

This document describes differences between V3 and previous ESP32 silicon wafer revisions.

Release Notes

Date	Version	Release notes
2020.01	V1.0	Initial release.

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1. Design Change in ECO V3

Espressif has recently released one wafer-level change on ESP32 Series of products (ECO V3). This document describes differences between V3 and previous ESP32 silicon wafer revisions. Below are the main design changes in ECO V3 Series of chips:

1. PSRAM Cache Bug Fix: Fixed “When the CPU accesses the external SRAM in a certain sequence, read & write errors can occur.”. Details of the issue can be found in item 3.9 in [ESP32 ECO and Workarounds for Bugs](#).
2. Fixed “When each CPU reads certain different address spaces simultaneously, a read error can occur.” Details of the issue can be found in item 3.10 in [ESP32 ECO and Workarounds for Bugs](#).
3. Optimized 32.768 KHz crystal oscillator stability, the issue was reported by client that there is a low probability that under ECO V1 hardware, the 32.768 KHz crystal oscillator couldn't start properly.
4. Fixed Fault injection issues regarding secure boot and flash encryption are fixed. Reference: [Security Advisory concerning fault injection and eFuse protections \(CVE-2019-17391\)](#) & [Espressif Security Advisory Concerning Fault Injection and Secure Boot \(CVE-2019-15894\)](#)
5. Improvement: Changed the minimum baud rate supported by the CAN module from 25 kHz to 12.5 kHz.



2. Impact on Customer Projects

This section is intended to help our customers to understand the impact of using ECO V3 in a new design or replacing older version SoC with ECO V3 in existing design.

2.1. Use Case 1: Hardware and Software Upgrade

This is the use-case where the new project is being initiated or upgrade for hardware and software in an existing project is a possible option. In such a case, the project can benefit from protection against fault injection attack and can also take advantage of newer secure boot mechanism and PSRAM cache bug fix with slightly enhanced PSRAM performance.

1. Hardware Design Changes:

Please follow the latest [Espressif Hardware Design Guideline](#). For 32.768 KHz crystal oscillator stability issue optimization, please refer to Section *Crystal Oscillator* for more information.

2. Software Design Changes:

- 1) Select **Minimum configuration** to **Rev3**: Go to *menuconfig* > **Component config** > **ESP32-specific**, and set the **Minimum Supported ESP32 Revision option** to “**Rev 3**”.
- 2) **Software version**: Recommend to use RSA-based secure boot from IDF4.1 and later. IDF3.X Release version can also work with application with original secure boot V1.

2.2. Use Case 2: Hardware Upgrade Only

This is the use-case where customers have existing project which can allow hardware upgrade but software needs to remain the same across hardware revisions. In this case the project gets benefit of security to fault injection attacks, PSRAM cache bug fix and 32.768KHz crystal oscillator stability issue. The PSRAM performance continues to remain the same though.

1. Hardware Design Changes:

Please follow latest [Espressif Hardware Design Guideline](#).

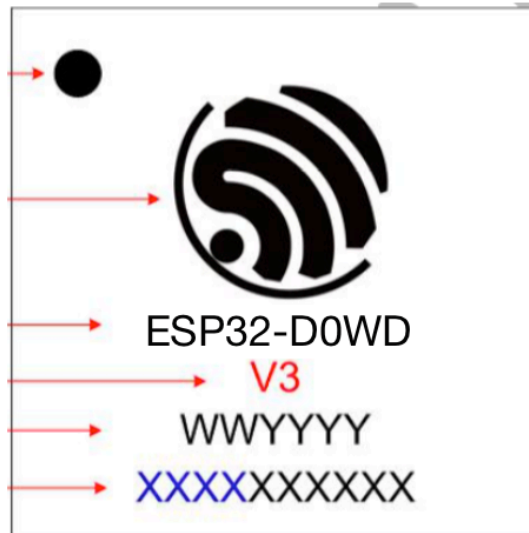
2. Software Design Changes:

Client can continue to use the same software and binary for deployed product. The same application binary will work on both ECO V1 and V3 chip versions.

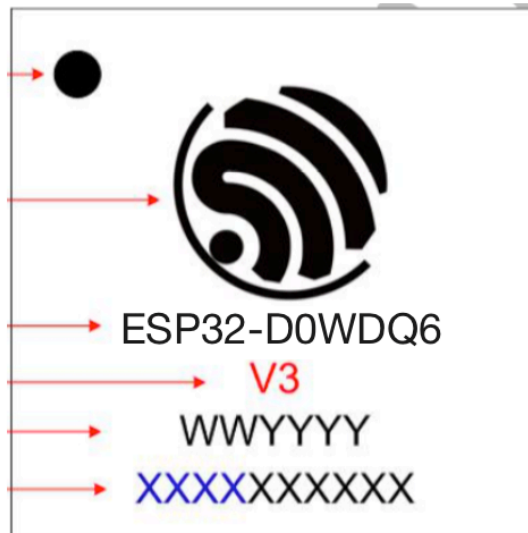


3. Label Specification

The label of ESP32-D0WD-V3 is shown below:



The label of ESP32-D0WDQ6-V3 is shown below:





4. Ordering Information

For product ordering, please refer to: [Espressif Products Ordering Information](#).



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